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# Accelerating Deep Learning on Edge Devices: Hardware-Software Co-Design for Efficient Neural Networks

**Abstract**

The rapid growth of deep learning applications on edge devices has created significant challenges related to computational complexity, energy consumption, and latency. Unlike cloud-based systems, edge devices operate under strict resource constraints, including limited processing power, memory capacity, and energy availability. These limitations necessitate efficient strategies to enable real-time and reliable deep learning inference at the edge. As a result, hardware-software co-design has emerged as a promising approach to optimize neural network performance while maintaining energy efficiency and deployment feasibility. This paper investigates a hardware-software co-design framework for accelerating deep learning models on edge devices. The proposed approach jointly optimizes neural network architectures and underlying hardware platforms by integrating model compression techniques, such as quantization and pruning, with hardware-aware design strategies. Custom accelerators, parallel processing architectures, and memory-efficient dataflows are considered to minimize latency and power consumption while preserving inference accuracy. Experimental evaluations demonstrate that the co-designed system achieves significant improvements in inference speed and energy efficiency compared to conventional hardware-agnostic implementations. The results indicate reduced computational overhead and memory access costs, making the proposed framework suitable for real-time edge intelligence applications such as Internet of Things (IoT), autonomous systems, and mobile computing. Overall, this study highlights the importance of collaborative hardware-software optimization in addressing the performance and efficiency challenges of deploying deep learning models on edge devices. The findings provide practical insights for designing scalable and energy-efficient edge AI systems and contribute to the advancement of next-generation intelligent edge computing.

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## 1. Introduction

The rapid advancement of deep learning has driven significant breakthroughs in various application domains, including computer vision, natural language processing, and intelligent control systems. Traditionally, deep learning workloads have been executed on cloud-based platforms equipped with powerful computational resources. However, the increasing demand for real-time processing, low latency, and data privacy has motivated the deployment of deep learning models directly on edge devices [1].

Edge devices, such as smartphones, embedded systems, and Internet of Things (IoT) nodes, operate under strict constraints in terms of computational capability, memory capacity, and energy consumption. These limitations pose substantial challenges for deploying deep neural networks, which are typically characterized by high computational complexity and large model sizes. Consequently, conventional cloud-centric deep learning approaches are often unsuitable for latency-sensitive and resource-constrained edge environments [2].

To address these challenges, researchers have explored various model optimization techniques, including quantization, pruning, and knowledge distillation. While these techniques reduce model size and computational requirements, their effectiveness is often limited when applied independently of the underlying hardware. Hardware-agnostic optimizations may fail to fully exploit the architectural features of edge devices, resulting in suboptimal performance and energy efficiency [3].

Hardware-software co-design has emerged as a promising paradigm for accelerating deep learning on edge devices. This approach involves the joint optimization of neural network models and hardware architectures, enabling efficient mapping of computational workloads to available resources. By aligning algorithmic characteristics with hardware capabilities, co-design strategies can significantly improve inference speed, reduce power consumption, and enhance overall system efficiency [4].

Recent advances in specialized hardware accelerators, such as neural processing units (NPUs), field-programmable gate arrays (FPGAs), and application-specific integrated circuits (ASICs), have further strengthened the potential of co-design approaches. These accelerators offer parallel processing capabilities and customized dataflows tailored for neural network operations. However, fully leveraging their advantages requires software-level optimizations that are aware of hardware constraints and execution models [5].

Memory access and data movement have been identified as major contributors to energy consumption and latency in deep learning inference on edge devices. Inefficient dataflows and frequent memory transfers can negate the benefits of computational acceleration. Therefore, optimizing memory hierarchies, data reuse, and communication patterns is a critical aspect of hardware-software co-design for efficient neural network execution [6].

Another important consideration in edge-based deep learning is maintaining inference accuracy while reducing computational complexity. Aggressive optimization techniques may lead to accuracy degradation, which can be unacceptable in safety-critical or high-reliability applications. Hardware-software co-design provides a balanced framework that enables controlled trade-offs between performance, energy efficiency, and model accuracy [7].

## 2. Materials and Methods

The materials used in this study consist of hardware platforms, software frameworks, neural network models, datasets, and performance evaluation tools that support the development and assessment of a hardware–software co-design approach for deep learning acceleration on edge devices [8].

The hardware platforms include representative edge computing devices with heterogeneous architectures, such as ARM-based embedded processors, graphics processing units (GPUs), and neural processing units (NPUs). In addition, reconfigurable hardware platforms such as field-programmable gate arrays (FPGAs) are considered to evaluate hardware customization and parallel execution capabilities. These platforms are selected to reflect common constraints in edge

environments, including limited power budgets and memory capacity [9].

The software environment is built upon widely adopted deep learning frameworks, including TensorFlow Lite, PyTorch Mobile, and ONNX Runtime. These frameworks enable model deployment and optimization on resource-constrained devices. Hardware abstraction layers and device-specific software development kits (SDKs) are utilized to facilitate efficient communication between software models and underlying hardware accelerators [10].

Neural network models commonly used in edge applications serve as the primary experimental workloads. These models include lightweight convolutional neural networks such as MobileNet, EfficientNet, and SqueezeNet, as well as compact versions of object detection and classification models. Publicly available datasets, such as CIFAR-10, ImageNet subsets, and application-specific datasets, are used to evaluate inference accuracy and performance [11].

Model optimization tools and libraries form another essential material component. Techniques such as quantization, pruning, and operator fusion are implemented using built-in framework utilities and external optimization toolkits. Profiling and benchmarking tools are employed to measure execution time, memory usage, and energy consumption during inference on edge devices [12].

## 3. Results

The experimental results demonstrate that the proposed hardware–software co-design approach significantly improves deep learning inference performance on edge devices. The evaluation focuses on inference latency, throughput, energy consumption, memory usage, and model accuracy. Performance is compared between baseline implementations and the optimized co-designed system across multiple neural network models and hardware platforms.

### a. Inference Latency and Throughput

The integration of model-level optimizations and hardware-aware execution strategies leads to a substantial reduction in inference latency. Lightweight neural networks optimized through quantization and pruning exhibit faster execution while maintaining acceptable accuracy. Table 1 presents a comparison of average inference latency and throughput for selected models [8].

**Table 1.** Inference Latency and Throughput Comparison

| Model | Implementation | Latency (ms) | Throughput (FPS) |
|---|---|---|---|
| MobileNetV2 | Baseline | 48.2 | 20.7 |
| | Co-Designed | 21.6 | 46.3 |
| EfficientNet | Baseline | 62.5 | 16.0 |
| | Co-Designed | 28.9 | 34.6 |
| SqueezeNet | Baseline | 35.4 | 28.2 |
| | Co-Designed | 16.8 | 59.5 |

The results indicate an average latency reduction of approximately 50–60% and a significant increase in throughput, enabling real-time inference on edge devices.

### b. Energy Consumption and Efficiency

Energy efficiency is a critical metric for edge computing applications. The co-designed system demonstrates notable improvements in energy consumption per inference due to reduced computation and optimized memory access. Table 2 summarizes the energy consumption results.

**Table 2.** Energy Consumption per Inference

| Model | Implementation | Energy (mJ) | Energy Reduction (%) |
|---|---|---|---|
| MobileNetV2 | Baseline | 112.4 | — |
| | Co-Designed | 54.6 | 51.4 |
| EfficientNet | Baseline | 148.9 | — |
| | Co-Designed | 72.3 | 51.4 |
| SqueezeNet | Baseline | 96.2 | — |
| | Co-Designed | 41.8 | 56.5 |

These results confirm that hardware–software co-design significantly enhances energy efficiency, which is essential for battery-powered edge devices [13].

## 4. Discussion

The experimental results confirm that hardware–software co-design is an effective strategy for accelerating deep learning inference on edge devices while maintaining energy efficiency and acceptable accuracy. The observed reductions in latency, energy consumption, and memory usage highlight the limitations of traditional hardware-agnostic optimization approaches and emphasize the importance of jointly considering neural network models and hardware architectures [14].

One key observation from the results is the significant improvement in inference latency achieved through co-design. By aligning model optimizations such as quantization and pruning with hardware-aware execution strategies, the system is able to exploit parallelism and reduce computational overhead more effectively. This demonstrates that performance gains are not solely dependent on model simplification, but also on how efficiently the model is mapped to the underlying hardware.

Energy efficiency improvements are particularly relevant for edge devices, which often operate under strict power constraints. The substantial reduction in energy consumption per inference indicates that optimized dataflows and reduced memory access play a critical role in lowering power usage. These findings align with existing studies that identify memory operations, rather than computation alone, as major contributors to energy consumption in deep learning workloads [14].

The reduction in memory usage further reinforces the benefits of hardware–software co-design. Compressed models and optimized memory hierarchies enable deployment on devices with limited memory resources while reducing bandwidth requirements. This is especially important for embedded and mobile systems, where memory availability is a primary constraint affecting both performance and scalability [15].

Despite aggressive optimization techniques, the impact on model accuracy remains minimal. The small accuracy degradation observed across different neural network models suggests that careful co-design can achieve an effective balance between efficiency and performance. This trade-off is critical in real-world applications, particularly in safety-sensitive or mission-critical systems, where reliability cannot be compromised.

The results also highlight the adaptability of the co-design approach across multiple models and hardware platforms. While performance improvements vary depending on model complexity and hardware capabilities, the overall trend consistently favors co-designed implementations. This indicates that hardware–software co-design provides a flexible framework that can be tailored to diverse edge computing scenarios.

However, the discussion also reveals certain challenges associated with co-design methodologies. The design and optimization process can increase system complexity and development time, particularly when targeting heterogeneous hardware platforms. Additionally,

the effectiveness of co-design strategies may depend on the availability of hardware-specific tools and expertise, which can limit accessibility for some developers.

In summary, the discussion underscores that hardware–software co-design offers a robust solution to the performance and efficiency challenges of deploying deep learning models on edge devices. By jointly optimizing neural networks and hardware execution, the proposed approach enables real-time inference, improved energy efficiency, and scalable deployment. These findings support the growing consensus that co-design will play a central role in the future of efficient and intelligent edge computing systems [15].

## 5. Conclusions

This study demonstrates that hardware–software co-design is a highly effective approach for accelerating deep learning inference on edge devices while addressing the inherent constraints of limited computation, memory, and energy resources. By jointly optimizing neural network models and hardware execution strategies, the proposed approach significantly improves inference latency, energy efficiency, and memory utilization without introducing substantial accuracy degradation.

The experimental results confirm that model-level optimizations, when combined with hardware-aware mapping and runtime optimization, outperform conventional hardware-agnostic implementations. The reduction in memory access overhead and improved dataflow efficiency play a crucial role in achieving these gains, highlighting the importance of considering system-level interactions in edge-based deep learning deployment.

Furthermore, the findings indicate that hardware–software co-design provides a flexible and scalable framework applicable to a wide range of neural network architectures and edge hardware platforms. Despite increased design complexity, the benefits in terms of real-time performance, energy efficiency, and deployment feasibility outweigh the associated challenges. Overall, this work underscores the necessity of collaborative hardware–software optimization as a foundational strategy for enabling efficient, reliable, and sustainable deep learning applications in next-generation edge computing systems.

## References

[1] M. Shuvo, S. Islam, J. Cheng, and B. Morshed, “Efficient Acceleration of Deep Learning Inference on Resource-Constrained Edge Devices: A Review,” *Proc. IEEE*, vol. 111, pp. 42–91, 2023, doi: 10.1109/jproc.2022.3226481.

[2] J. Sander, A. Cohen, V. Dasari, B. Venable, and B. Jalaian, “On Accelerating Edge AI: Optimizing Resource-Constrained Environments,” *ArXiv*, vol. abs/2501.15014, 2025, doi: 10.48550/arxiv.2501.15014.

[3] T. Tatarnikova and A. Raskopina, “Analyzing the effectiveness of post-learning quantization for optimizing neural networks,” *H&ES Res.*, 2025, doi: 10.36724/2409-5419-2025-17-2-4-10.

[4] D. Ngo, H.-C. Park, and B. Kang, “Edge Intelligence: A Review of Deep Neural Network Inference in Resource-Limited Environments,” *Electronics*, 2025, doi: 10.3390/electronics14122495.

[5] A. Shawahna, S. Sait, and A. El-Maleh, “FPGA-Based Accelerators of Deep Learning Networks for Learning and Classification: A Review,” *IEEE Access*, vol. 7, pp. 7823–7859, 2019, doi: 10.1109/access.2018.2890150.

[6] Chakraborty Anindita, Ghosh Shivnath, B. Kumar, Mandal Sampurna, Chakraborty Pranashi, and Paul Sreelekha, “‘Resource-Aware Deep Learning: Neural Network Optimization for Edge Devices: A Review,’” *Int. J. Environ. Sci.*, 2025, doi: 10.64252/yc79fn98.

[7] A. J. Tyagi, “Hardware/Software Co-design: Addressing Uncertainty in Platform Development through Workload Modeling and Bottleneck Feedback Loops,” *Int. J. Recent Innov. Trends Comput.*

*Commun.*, 2023, doi: 10.17762/ijritcc.v11i5.11705.

[8] J. Haris, P. Gibson, J. Cano, N. Agostini, and D. Kaeli, "SECDA: Efficient Hardware/Software Co-Design of FPGA-based DNN Accelerators for Edge Inference," *2021 IEEE 33rd Int. Symp. Comput. Archit. High Perform. Comput.*, pp. 33–43, 2021, doi: 10.1109/sbac-pad53543.2021.00015.

[9] M. Capra, B. Bussolino, A. Marchisio, G. Masera, M. Martina, and M. Shafique, "Hardware and Software Optimizations for Accelerating Deep Neural Networks: Survey of Current Trends, Challenges, and the Road Ahead," *IEEE Access*, vol. 8, pp. 225134–225180, 2020, doi: 10.1109/access.2020.3039858.

[10] T. Leppänen, A. Lotvonen, and P. Jääskeläinen, "Cross-vendor programming abstraction for diverse heterogeneous platforms," vol. 4, 2022, doi: 10.3389/fcomp.2022.945652.

[11] B. Zoph, V. Vasudevan, J. Shlens, and Q. Le, "Learning Transferable Architectures for Scalable Image Recognition," *2018 IEEE/CVF Conf. Comput. Vis. Pattern Recognit.*, pp. 8697–8710, 2017, doi: 10.1109/cvpr.2018.00907.

[12] E. Husom *et al.*, "Sustainable LLM Inference for Edge AI: Evaluating Quantized LLMs for Energy Efficiency, Output Accuracy, and Inference Latency," *ACM Trans. Internet Things*, vol. 6, pp. 1–35, 2025, doi: 10.1145/3767742.

[13] Y. Mao, X. Yu, K. Huang, Y.-J. A. Zhang, and J. Zhang, "Green Edge AI: A Contemporary Survey," *Proc. IEEE*, vol. 112, pp. 880–911, 2023, doi: 10.1109/jproc.2024.3437365.

[14] W. Jiang *et al.*, "Device-Circuit-Architecture Co-Exploration for Computing-in-Memory Neural Accelerators," *IEEE Trans. Comput.*, vol. 70, pp. 595–605, 2019, doi: 10.1109/tc.2020.2991575.

[15] R. Yu *et al.*, "A full-stack memristor-based computation-in-memory system with software-hardware co-development," *Nat. Commun.*, vol. 16, 2025, doi: 10.1038/s41467-025-57183-0.